Fabrication of 60-nm transistors on 4-in. wafer using nanoimprint at all lithography levels

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Nanoimprint lithography (NIL) is a paradigm-shift method that has shown sub-10-nm resolution, high throughput, and low cost. To make NIL a next-generation lithography tool to replace conventional lithography, one must demonstrate the needed overlay accuracy in multilayer NIL, large-area uniformity, and low defect density. Here, we present the fabrication of 60-nm channel metal–oxide–semiconductor field-effect transistors on whole 4-in. wafers using NIL at *all* lithography levels. The nanotransistors exhibit excellent operational characteristics across the wafer. The statistics from consecutive multiwafer processing show an average overlay accuracy of 500 nm over the entire 4-in. wafer. The accuracy is much better when the field size is reduced. The overlay accuracies are limited by the current alignment method and can be improved substantially. The work presents a significant advance in nanoimprint development and its applications in manufacturing of integrated electrical, optical, chemical, and biological nanocircuits. © *2003 American Institute of Physics.* [DOI: 10.1063/1.1600505]

Lithography, a key step in defining the size of micro/nanodevices, is a critical tool for microchip manufacturing. Conventional lithography creates features based on the principle of using a radiation (e.g., light) to locally modify the chemical structure of a resist. As the microchip feature size shrinks 30% every three years, following Moore's law, the radiation wavelength used in a conventional lithography tool must be reduced accordingly. However, a short wavelength requires significant and often fundamental changes in the lithography tools (e.g., lens materials and designs), masks, and resist materials. These changes, even if possible, would take substantial time and resources to develop. Hence, it is still unclear which lithography methods can be used beyond the 90-nm feature-size node that is presently achieved by using 193-nm wavelength radiation and phase masks.

Nanoimprint lithography (NIL)[1] has a working principle fundamentally different from conventional lithography. Nanoimprint creates features by a mechanical deformation of the resist shape using a mold. During the deformation, a nanoimprint resist (made of a thermal-plastic or a curable material) is in a liquid flowable state and becomes solidified after the deformation.[1–4] NIL has demonstrated sub-10-nm resolution, which is primarily determined by the molecular size and the mechanical strength of the resist.[5,6] NIL has shown high throughput (less than 60 s per wafer) due to its parallel process. And it should be low cost,[5,6] since NIL does not use sophisticated lenses and radiation source. Furthermore, for semiconductor integrated circuit (IC) manufacturing, NIL can be the lithography used for all future (seven) feature nodes all the way down to 5 nm, without changing the lithography tools, resists, and masks, which would be required in conventional lithography.

Despite its very impressive progress, to show that NIL can be a next-generation lithography to replace conventional lithography in IC manufacturing, NIL must demonstrate the needed overlay accuracy, large-area uniformity, and low defect density. Previously, only two-layer NIL alignment on surface topology was achieved.[7] In this letter, we show the fabrication of operational 60-nm metal–oxide–semiconductor field-effect transistors (MOSFETs) over the entire 4-in. wafer using nanoimprint at all lithography levels. We will describe the device design and fabrication, detailed NIL, electrical performance, as well as alignment data and analysis.

The nanotransistors were designed to have four lithographical layers to form the active area, gate, via, and metal contact, as shown in Fig. 1. The fabrication process was a standard self-aligned four-mask MOSFET process (Fig. 1). All lithography levels were performed by NIL. In fabrication, 4-in. *p*-type silicon wafers were used as device substrates. The first NIL defined the active areas of nano-MOSFETs. Next, the patterns were transferred into the underneath Si_3N_4 layer by CHF_3 reactive ion etching (RIE). A local oxidation of silicon process was performed to isolate individual devices. After removing Si_3N_4, a diluted HF dip was performed to etch the isolation oxide back to have an even surface across the wafer. The active area was doped with boron. A 10-nm gate oxide was grown by dry oxidation. A 170-nm polycrystalline silicon layer was deposited as gate material. The second NIL defined the gates of nano-MOSFETs. The polycrystalline silicon gates were made by Cr lift-off and Cl_2 RIE with Cr as etching mask. After the gate formation, the sources and drains were doped heavily with arsenic, followed by a 90-nm plasma-enhanced chemical vapor deposition of SiO_2 as a passivation. The third NIL defined the vias of nano-MOSFETs. The via holes were etched through passivation SiO_2 by CHF_3 RIE. Ti (40 nm) was filled into the holes by e-beam evaporation and lift-off. The fourth NIL defined the metal contacts of nano-

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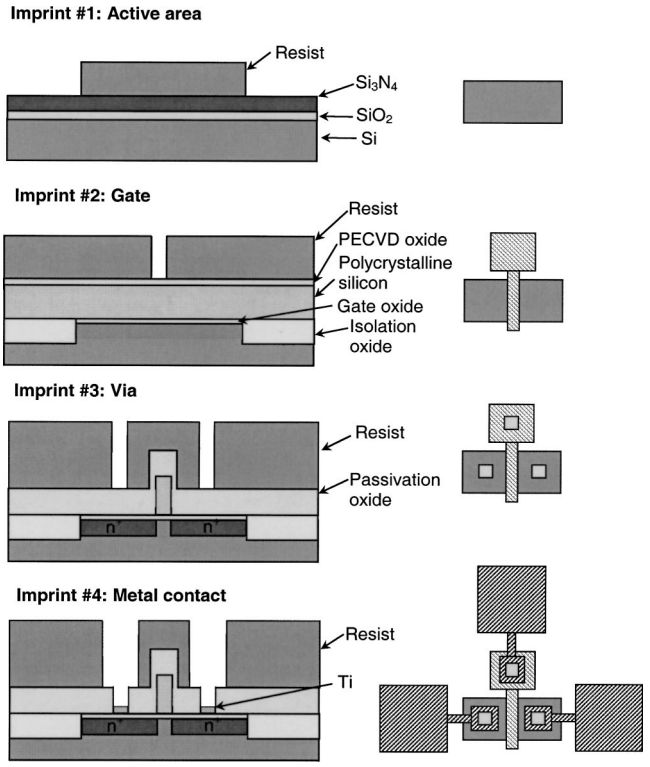


FIG. 1. The cross-section schematics of the nano-MOSFETs fabrication using NIL at all (four) lithographic levels (left) and the top view of the four-level patterns (right). (Imprint #1: active area; Imprint #2: gate; Imprint #3: via; Imprint #4: metal contact.)

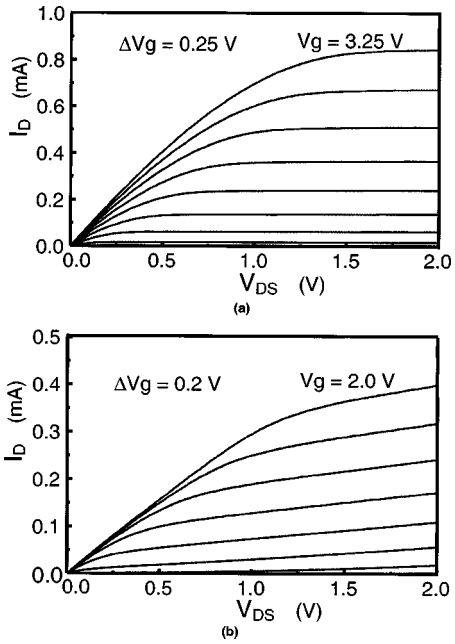


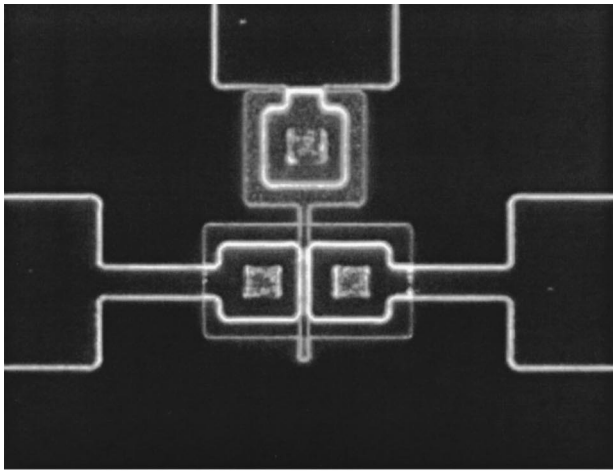
FIG. 2. The $I-V$ measurements of the MOSFETs fabricated by using NIL at all (four) lithographic levels to demonstrate that they are working. (a) The 1-μm-gate-length MOSFET ($V_t = 1.25$ V). (b) The 60-nm-channel-length MOSFET ($V_t = 0.8$ V, $S = 86$ mV/decade).

MOSFETs. The metal contact layer of 140-nm Al was fabricated by e-beam evaporation and lift-off. Finally, the completed devices were sintered in H_2/N_2 ambient. It should be pointed out that in the third and fourth lithography layers, the imprints were carried out over a nonflat surface.

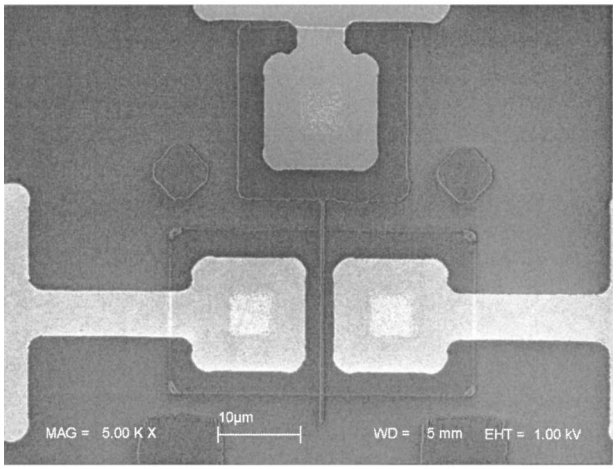
The details of NIL processes are as follows. NIL resist was a thermal-plastic polymer made in house. To avoid the misalignment caused by thermal expansion during NIL, we used Si wafer as the mask (also called mold) which has an identical thermal expansion as the Si substrate. The multilayer NILs were carried out on a tool developed in house. The NIL tool consists of a modified commercial contact aligner, a transportation holder, and a home-built imprinting machine. The Si mask and the Si wafer are aligned and contacted on the aligner, are then kept in alignment with mechanical clamps on the holder and transported onto the imprinting machine for imprinting.[7] To avoid any shift and rotation between the mask and the wafer, a very uniform pressing force is applied on the mask and the wafer for imprinting. The very uniform pressing force creates uniformity of imprinting over a large area. To align the Si mask and Si wafer, an image processing technique called as ''back-side alignment'' (BSA) is used by the aligner. In BSA, the wafer was inserted first and its alignment mark image was grabbed by a microscope camera, followed by inserting the mask and aligning the aligning marks on the back side of the mask with the grabbed images of aligning marks on the wafer. The SiO_2 patterns on the masks for NIL were produced by photolithography or electron-beam lithography (EBL) and RIE of SiO_2. Photolithography was used to make the patterns larger than 1 μm. EBL was used to make the submicron patterns that were the gates of nano-MOSFETs. The NIL masks were double-side polished Si substrates for better aligning mark image quality.

The $I-V$ measurements of the nano-MOSFETs over entire 4-in. wafer have demonstrated that the devices were operating properly. Figure 2(a) was the measurement of a 1-μm-gate-length MOSFET. The device had a threshold voltage of 1.25 V. Figure 2(b) was the measurement of a 60-nm-channel-length MOSFET. The MOSFET had a channel doping concentration of 5×10^{17} cm^{-3}, source/drain junction depth of 100 nm, and gate length of 200 nm. The 60-nm channel length was estimated by gate length minus [$2\times(0.7\times$source/drain junction depth)]. (Note: Lateral diffusion of source/drain ion implantation is 0.7 times source/drain junction depth.) The device had a threshold voltage of 0.8 V and a subthreshold slope swing 86 mV/decade. The fabrication of these devices has achieved a submicron overlay accuracy. In Fig. 3, the optical image (dark field) of 1-μm gate length MOSFET (a) and the scanning electron microscope (SEM) image of a 60-nm-channel-length MOSFET (b) were shown. From the images, we can see that overlay accuracies among the four layers were all within 0.5 μm in both X and Y directions. The overlay accuracy was also confirmed by the measurement of nearby aligning marks.

The overlay accuracy of the nano-MOSFETs fabrications over the 4-in. wafer has been studied extensively. The overlay accuracies between different NIL lithography levels were measured at nine locations over each 4-in. wafer for each lithography run. These locations were uniformly distributed along a ~4-cm-radius circle from the wafer center, as shown at the top of Fig. 4. The overlay accuracy was measured using venier-type aligning marks formed with the two adjacent imprinted layers. The venier was formed by two gratings of period 18 and 18.5 μm, respectively, that clearly show a 0.5-μm misalignment, hence giving a measurement accuracy of 0.25 μm through visual estimation.

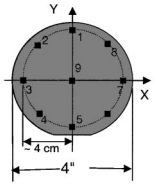


(a)



(b)

FIG. 3. The images of the MOSFETs fabricated by using NIL at all (four) lithographic levels. (a) Dark-field optical image of a 1-μm-gate-length MOSFET. (b) The SEM image of a 60-nm-channel-length MOSFET. (Note: The overlay accuracy among the layers is within 0.5 μm in both X and Y directions in the images.)



Data in X-Direction: (μm)

Run #	1	2	3	4	5	6	7	8	9	Ave_s	σ_s
1	-1	-0.5	0	+0.25	+0.5	0	-0.5	-1	-0.5	**0.5**	**0.3**
2	+1	+1	+0.5	0	-0.5	-0.5	0	+1	+0.5	**0.5**	**0.4**
3	+1.5	+1.5	+1	0	-0.5	0	+0.5	+1	+0.5	**0.8**	**0.6**
4	-1	-1	-0.5	-0.5	0	-0.5	-0.5	-0.5	-0.5	**0.5**	**0.3**
5	-0.5	-0.5	-0.5	-0.5	-0.5	-0.5	0	0	0	**0.3**	**0.2**
6	+0.25	0	+0.5	+1	+0.75	+0.5	+0.5	0	+0.5	**0.4**	**0.3**
7	-1	-1	-0.5	0	+0.25	0	-0.5	-1	-0.25	**0.5**	**0.4**
8	+0.5	0	-0.5	-0.5	+0.5	-0.5	-0.5	+0.25	-0.25	**0.3**	**0.2**
Ave_{multi}	**0.7**	**0.7**	**0.6**	**0.4**	**0.6**	**0.4**	**0.4**	**0.6**	**0.5**	**0.5**	
σ_{multi}	**0.3**	**0.5**	**0.4**	**0.4**	**0.2**	**0.3**	**0.4**	**0.4**	**0.3**	**0.2**	

Data in Y-Direction: (μm)

Run #	1	2	3	4	5	6	7	8	9	Ave_s	σ_s
1	+1.5	+1	+1.25	+1.25	+1.5	+1.5	+2	+1.5	+1.5	**1.3**	**0.4**
2	-0.5	-0.5	0	0	-0.5	-0.5	-1	+1	-0.5	**0.6**	**0.3**
3	+1	+1	+1.5	+1.5	+1	0	0	0	+0.5	**0.7**	**0.6**
4	+1	+1	+1	+1.5	+1.5	+1.5	+1.5	+1.5	+1	**1.2**	**0.2**
5	0	0	0	0	0	-0.5	0	0	0	**0.1**	**0.2**
6	0	0	0	0	0	0	0	0	0	**0**	**0**
7	+0.5	0	0	0	0	+0.5	+1	+1	+0.25	**0.4**	**0.3**
8	0	0	0	0	0	-0.5	-0.5	-0.5	0	**0.2**	**0.2**
Ave_{multi}	**0.7**	**0.6**	**0.6**	**0.6**	**0.6**	**0.8**	**0.9**	**0.8**	**0.6**	**0.6**	
σ_{multi}	**0.5**	**0.5**	**0.6**	**0.6**	**0.6**	**0.6**	**0.7**	**0.6**	**0.5**	**0.5**	

FIG. 4. The overlay accuracies and the statistics of all (eight) consecutive lithography runs for multilayer NIL in the nano-MOSFETs fabrications. The data came from two finished wafers and one unfinished wafer. The numbers in the first row of the table are corresponding to the nine locations over the 4-in. wafer shown in the top schematic. The overall statistical average is 0.5 μm with a standard deviation of 0.2 μm in the X-direction, and 0.6 μm with a standard deviation of 0.5 μm in the Y-direction.

The overlay measurements of all (eight) runs of multilayer NIL in the nano-MOSFETs fabrications are shown in Fig. 4. The eight consecutive runs of multilayer NIL came from the fabrications of two finished wafers and one unfinished wafer. Each row of the tables in Fig. 4 gives the overlay accuracies at the nine locations of a 4-in. wafer for a lithography run, which are illustrated at the top of Fig. 4. The last two columns of the tables give the statistical average and standard deviation of the nine locations for each run. The last two rows of the tables give the statistical average and standard deviation of all runs on the same location. From the top table of data in the X direction, all (eight) runs had the statistical average over the 4-in. wafer of less than 1 μm. This indicated a 100% possibility of achieving submicron overlay accuracy over the 4-in. wafer in the X direction. From the bottom table of data in the Y direction, six runs out of all (eight) runs had a statistical average over the 4-in. wafer of less than 1 μm. This indicated a 75% possibility of achieving submicron overlay accuracy over the 4-in. wafer in the Y direction. The possibility difference between X and Y directions was due to statistics variation of less total run number. Finally, at the right-bottom corner of these tables, the statistical average and standard deviation of all data were calculated. The overall statistics gave a statistical average 0.5 μm with a standard deviation of 0.2 μm in the X direction, and a statistical average 0.6 μm with a standard deviation of 0.5 μm in the Y direction. The statistics study shows that an average overlay accuracy of $\sim$500 nm over the entire 4-in. wafer has been demonstrated.

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